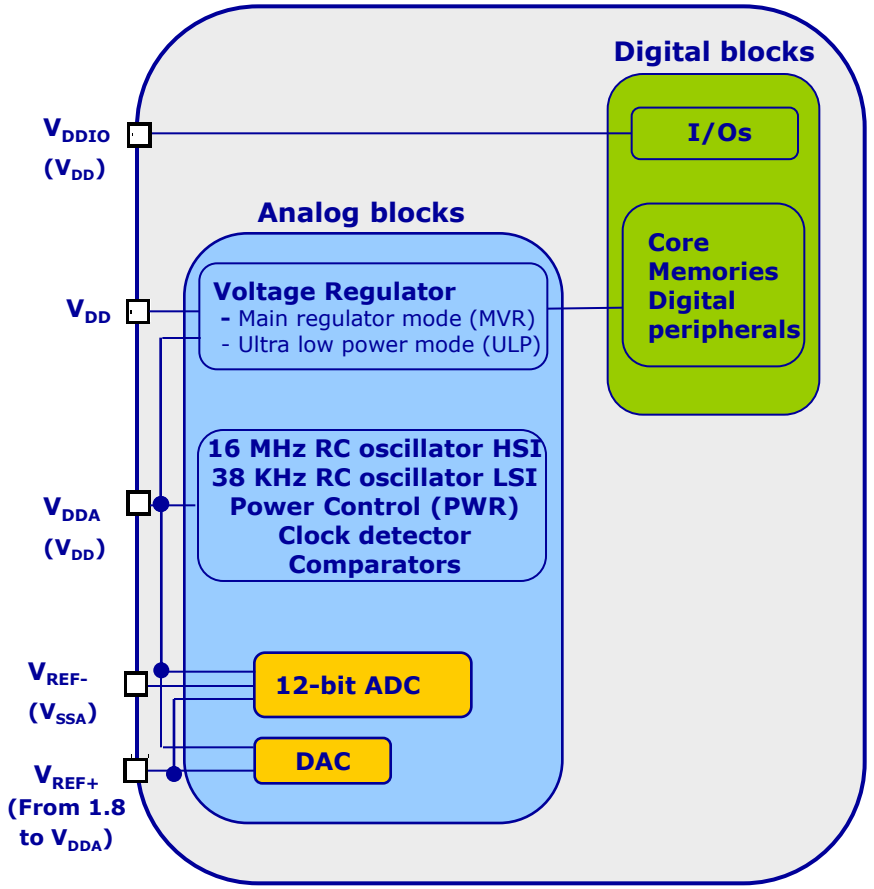
Power and Reset

Power Supply

- **Power Supply Schemes**
  - **VSS** ; **VDD** = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through VDD pins, the corresponding ground pin is VSS.
  - **VSSA** ; **VDDA** = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to VDDA is 1.8 V when the ADC1 is used). VDDA and VSSA must be connected to VDD and VSS, respectively.
  - **VSSIO** ; **VDDIO** = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. VDDIO and VSSIO must be connected to VDD and VSS, respectively.
  - **VREF+** ; **VREF-** (for ADC): external reference voltage for ADC. Must be provided externally through VREF+ and VREF- pin. VREF+ in the range 1.8V to VDDA
  - **VREF+** (for DAC): external voltage reference for DAC must be provided externally through VREF+.

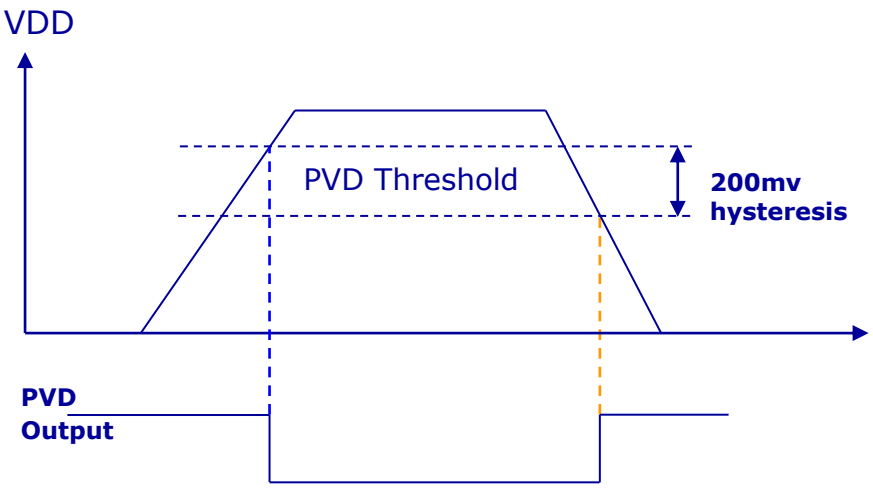


Supply monitoring and Reset circuitry

- **Full Reset circuitry / Supply Monitoring**
  - Power On Reset (POR) / Power Down Reset (PDR) “ZERO Power” - always ON
  - Brown Out detection (BOR) - Can be ON/OFF in Low Power modes
  - Programmable Voltage Detection (PVD) - Can be ON/OFF
  - Extended battery lifetime down to 1.65V at power down if no BOR

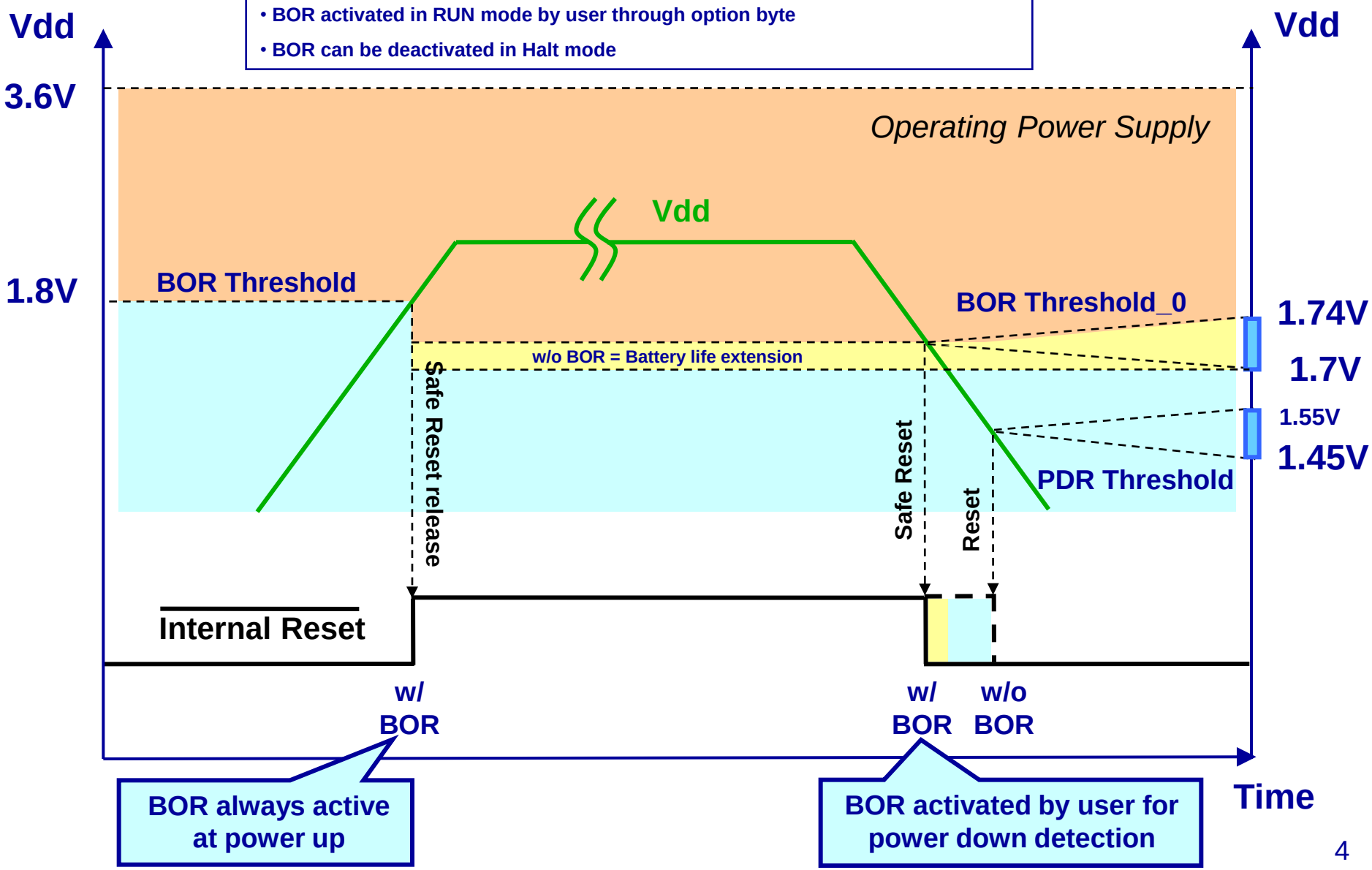
- **Programmable Voltage Detector (PVD)**
  - Enabled by software
  - Monitor the VDD vs. PVD threshold
  - Threshold configurable from 1.85V to 3.05V by step of 200mV + One pin used as external threshold
  - Generate interrupt if enabled when VDD < Threshold or VDD > Threshold

  ➔ Can be used to generate a warning message and/or put the MCU into a safe state



Supply monitoring w/ or w/o Brown Out Reset

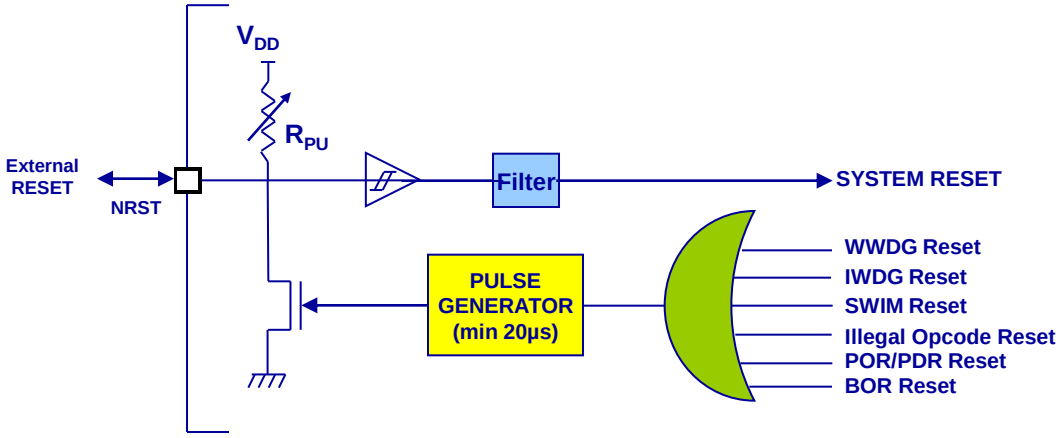
- BOR complies w/ ALL Vdd rise/fall time = No constraints on power supply shape
- BOR activated in RUN mode by user through option byte
- BOR can be deactivated in Halt mode



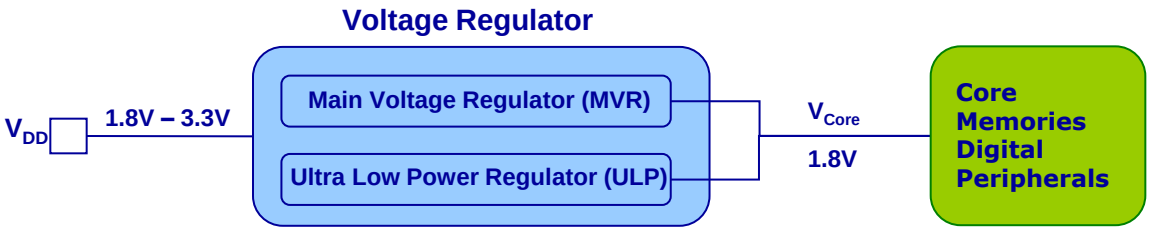
Reset sources

- **External RESET**
  - A negative **reset pulse** larger than **300ns** on NRST pin generates an internal reset system.
  - NRST pin is also an **open-drain output** which delivers a **minimum pulse of 20µs** controlled by internal temporization.
  - There is an **internal weak pull-up** to maintain the reset pin at 1 when reset is not forced. It avoids spurious reset
  - NRST pin can be configured as a **general purpose push-pull output** (PA1) only once → the MCU can be reset only by software or PDR reset or other internal reset source.

- **Internal RESET**
  - WWDG end of count condition
  - IWDG end of count condition
  - Swim block request from external device
  - Illegal Opcode Reset
  - POR/PDR Reset
  - BOR reset



Voltage regulator



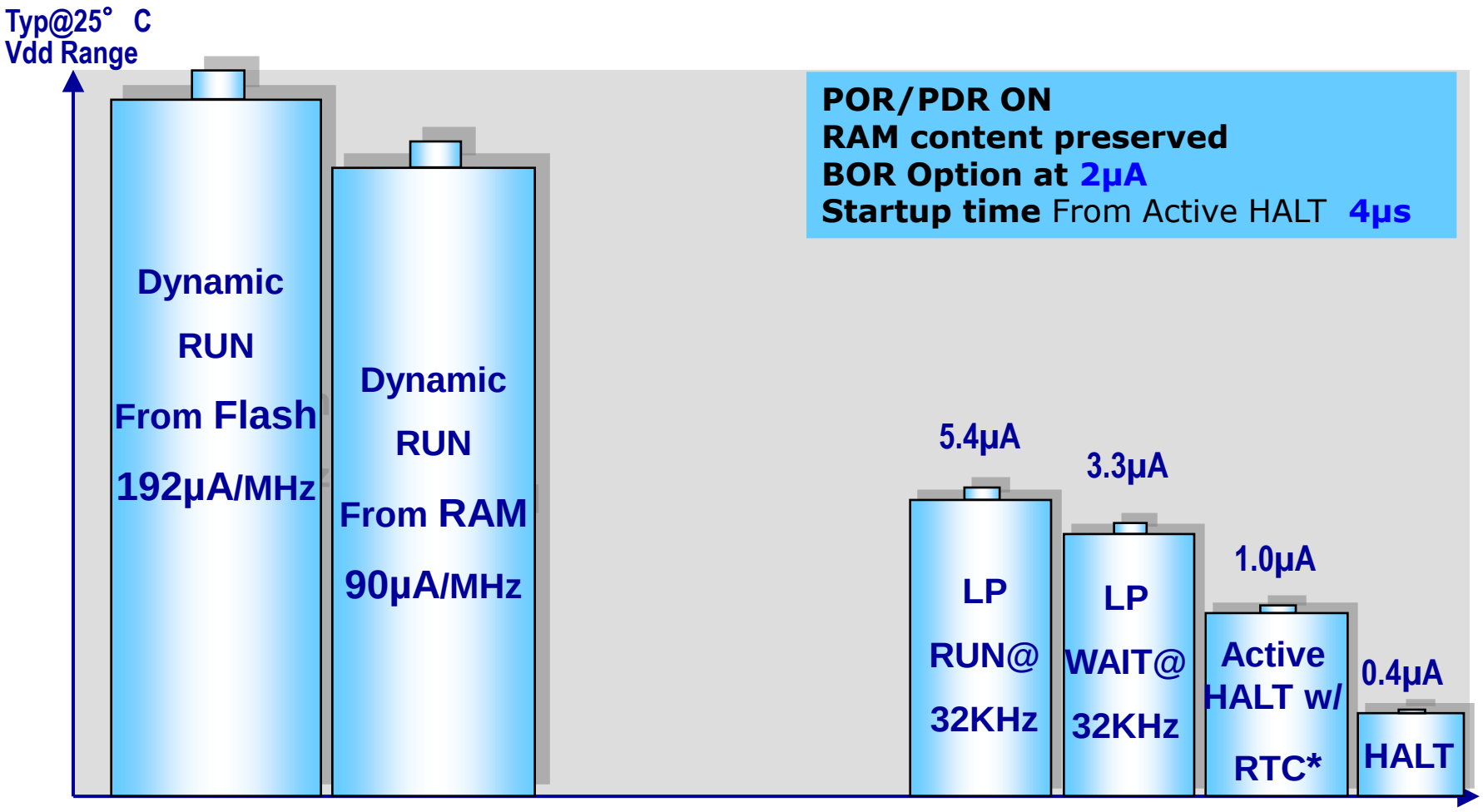
- The voltage regulator has two different modes:
  - Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
  - Ultra low power regulator mode (ULP) for Halt and Active-halt modes.

Low Power modes

- The STM8L15x devices supports 5 low power modes:

Mode		Features
Wait : - Wait for event (WFE) - Wait for interrupt (WFI)		- CPU is stopped, - Selected peripherals keep running. - Registers and RAM content are preserved, - Clock configuration remain unchanged
Low Power Run NEW		- CPU is still running - Flash, data EEPROM, voltage regulator and all peripherals are stopped except RTC and one other peripheral - Execution is done from RAM with a Low Speed Oscillator
Low Power Wait NEW		- CPU is stopped - EEPROM is switched off and Regulator is put in Ultra Low Power mode, - All interrupt must be masked - RTC and one peripheral being active
Active HALT	RTC on	- High Speed clocks off, POR/PDR On, - RAM ON (registers' content preserved),
	AWU	- High Speed clocks off, - RTC fed by low speed internal RC, no accurate calendar function
HALT		- All clocks off, POR/PDR On, - RAM ON (registers' content preserved) - RTC OFF

Low Power consumption values



- **LP Wait mode:** LSI/LSE ON, peripherals can be activated
- **ACTIVE HALT mode:** All clocks OFF, RTC ON
- **HALT mode:** All clocks OFF, RTC OFF

- ***Also possible: RTC on LSI:** RTC feed by low speed internal RC, periodic wake up but no accurate calendar function*

Wait mode

- **Wait mode :** CPU stopped, peripherals and interrupt controller kept running

  - Entered by executing special instructions:
    - WFI (Wait For Interrupt)
      - Voltage regulator mode : MVR
      - Exit : all internal or external interrupt, reset → CPU services the interrupt and resumes processing
    - WFE (Wait For Event)
      - An event can be generated by timers, serial interfaces, DMA controller, comparators and I/O ports if enabled by WFE control registers
      - Voltage regulator mode : MVR
      - Exit :
        - Interrupts : CPU services the interrupt and goes back to WFE mode.
        - Wakeup event : CPU resumes processing → no context save/restore activity (this saves time and power consumption).

  - Further power consumption can be reduced by using this mode together with
    - Slowing down the system clock
    - Gating (PCG) the peripherals clocks when they are unused

Low Power Run / Wait modes

- **Low Power Run mode**
  - ***OFF***: EEPROM, High Speed Oscillators (HSI and HSE)
  - ***ON***: CPU, RTC and one peripheral, Low Speed Oscillator (LSI or LSE)
  - ***Execution*** is done from RAM with a Low Speed Oscillator (LSI or LSE)
  - ***Voltage regulator mode*** : ULP
  - ***Entered*** ***** by software sequence
  - ***Exit*** ***** by software sequence

- **Low Power Wait mode**
  - Low Power Run mode **but** with **CPU OFF**
  - ***Entered*** by executing a WFE instruction when MCU is in Low Power Run mode
  - ***Exit*** by external or internal events, reset
  - → The MCU returns to low power run mode

* see next slide

Low Power Run mode: Enter/Exit

- Entered by software sequence
  1. Jump to RAM
  2. Switch system clock (SYSCLK) to LSI or LSE clock sources
  3. Switch OFF all peripherals, oscillator (except LSI or LSE) and analog blocks (except RTC and one peripheral e.g. TIM1)
  4. Mask all interrupts
  5. Disable all non-maskable interrupt (NMI) sources
  6. Switch OFF the Flash/Data EEPROM
  7. Add a software delay loop to ensure Flash/Data EEPROM off status
  8. Configure the ultra low power mode for the regulator

- Exit by software sequence
  1. Switch ON the main regulator
  2. Switch ON the Flash/Data EEPROM
  3. Reset interrupt mask and enable the NMI if necessary
  4. Switch ON what is necessary and jump to Flash/Data EEPROM if needed.

Halt / Active Halt modes

- **Active Halt mode**
  - ***OFF***: CPU, peripheral clocks and High Speed Oscillators
  - ***ON***: Comparator**, IWDG, RTC/ LCD, BEEP still active if previously enabled (clocked by LSI or LSE), PVD, POR/PDR and BOR**
  - ***Voltage regulator mode*** : MVR / ULP depending on clock controller configuration
  - ***Entered*** by executing **HALT** instruction
  - ***Exit*** * External (from IOs) or RTC interrupts, reset and Comparator**
- **Halt mode**
  - ***OFF***: CPU, peripheral clocks and High & Low Speed Oscillators
  - ***ON***: Comparator**, IWDG, PVD, POR/PDR and BOR**
  - ***Voltage regulator mode*** : ULP
  - ***Entered*** by executing **HALT** instruction
  - ***Exit*** * External (from IOs) interrupts, reset and Comparator**

*, ** see next slide

Halt / Active Halt modes: fine tuning

** User can select to wakeup on HSI (Fast wakeup) or on the same clock source as that used before entering Halt or Active-halt mode is selected (selection is made through FHWU bit in CLK_ICKCR register).*

*** The Internal reference voltage can be switched off to further reduce power consumption (BOR and comparator will be OFF), selection done through ULP and FWU bits in PWR_CSR2 register*

<table>
<tr><th>ULP</th><th>FWU</th><th colspan="2">Consumption / Wakeup time in Halt/Active-halt</th></tr>
<tr><td>0</td><td>x</td><td colspan="2">Internal reference voltage always on
<u>0.4µA</u> + 2µA more
~6µs wakeup time</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Internal reference voltage OFF
0.4µA</td><td>Internal reference voltage wakeup time is added to wait until the internal reference voltage starts
~2ms wakeup time</td></tr>
<tr><td>1</td><td>1</td><td>Fast wakeup time is forced without waiting the start of the internal reference voltage.
In this case, the analog features do not work immediately after wakeup.
~6µs wakeup time</td></tr>
</table>

Low Power modes: summary

Low Power Modes	Entry	Functions							Low power modes names and consumptions	
		CPU	Periphs	High Speed Osc	RTC Calendar	LSI LSE	FLASH	RAM	STM8L Typical values @ 3V / 25°C	STM8L Typical values @ 3V / 85°C
LP RUN	**SW Sequence**	ON	Can be enabled	OFF	ON	ON	OFF	ON	**5.4µA**	
LP WAIT	**SW Sequence + WFE**	OFF	Can be enabled	OFF	ON	ON	OFF	ON	**3.3µA**	
ACTIVE Halt w/ full RTC	**HALT**	OFF			ON	ON	OFF	ON	**1.0µA***	**1.4µA**
ACTIVE Halt w/ RTC on LSI					OFF	ON	OFF	ON	**0.8µA***	**1.2µA**
Halt					OFF	OFF	OFF	ON	**0.4µA***	**1µA**

*** Internal reference voltage + BOR OFF**

Quiz

- What is the minimum V_{DD} value at power down when BOR disabled?

  _____

- How many PVD threshold levels are there?

  _____

- How many low power modes is there?

  _____

- What are the wake-up sources from WFE mode?

  _____

- How many reset sources are there?

  _____

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